REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-9, 11-33 and 35-50 are pending. Claims 1-9, 11-33 and 35-50 have been rejected.

Claims 4, 5, 20, 28 and 29 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Claim Objections

Claims 20 and 28 have been objected to because of informalities.

Applicants have amended claims 20 and 28 to overcome the Examiner's objection.

Rejections Under 35 U.S.C. § 102

Claims 11-24 and 35-48 have been rejected under 35 U.S.C. § 102(e) as being taught by U.S. Patent No. 6,446,198, to Sazegari ("Sazegari").

Claim 11 includes receiving a first vector having a plurality of numbers, and looking up simultaneously a plurality of elements of a second vector from the plurality of look-up tables, each of the plurality of elements being in one of the plurality of look-up tables and being pointed to by one of the plurality of numbers of the first vector.

Sazegari discloses a completely different method than claimed by Applicants. In fact, Sazigari discloses using a permute instruction to perform a number of look up operations on a single data table. More specifically, Sazegari discloses simultaneously performing a number of lookup operations in a single table using the value stored in the register (Figure 2, col. 3, line 64-line 3). In particular, Sazegari discloses a single table 34 that consists of two vectors, data 1 and data 2. The permute instruction is used to simultaneously read values from these two vectors

from a single table 34 in accordance with index values stored in register 36 (col. 4, lines 24-32, col. 4, lines 59-66).

Thus, Sazegari merely discloses simultaneously reading values of two vectors from a single table according to index values stored in the register. In contrast claim 11 refers to looking up simultaneously a plurality of elements of a second vector from the plurality of look-up tables, each of the plurality of elements being in one of the plurality of look-up tables and being pointed to by one of the plurality of numbers of a first vector.

Because Sazegari fails to disclose all limitations of claim 11, applicants respectfully submit that claim 11 is not anticipated under 35 U.S.C. § 102(e) by Sazegari.

Because claims 12-24, 35-48, and 50 contain related limitations, applicants respectfully submit that claims 12-24, 35-48, and 50 are not anticipated under 35 U.S.C. § 102(e) by Sazegari.

Rejections Under 35 U.S.C. § 103

Claims 1-9, 25-33 and 49 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Sazegari, in view of U.S. Patent No. 6,397,324 to Barry, et al. ("Barry") and further in view of U.S. Patent No. 5,768,628 to Priem ("Priem").

Claim 1 includes receiving a first vector having a first plurality of numbers and a second vector having a second plurality of numbers, each of the first plurality of numbers pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables.

Sazegari merely discloses a permute instruction that simultaneously reads values of two vectors from a single table in accordance with index values stored in a register (col. 4, lines 28-32). Thus, Sazegari merely discloses index values to read values of two vectors from a single table. In contrast, claim 1 refers to receiving a first vector having a first plurality of numbers,

each of the first plurality of numbers pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables.

Barry discloses splitting a general purpose register file into separate address and compute register files in a very long instruction word (VLIW) processor (Abstract), and similarly to Sazegari, fails to disclose receiving a first vector having a first plurality of numbers, each of the first plurality of numbers pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables, as recited in claim 1.

Priem discloses storing wave tables in system memory (Abstract), and similarly to Sazegari and Barry, fails to disclose receiving a first vector having a first plurality of numbers, each of the first plurality of numbers pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables, as recited in claim 1.

It is respectfully submitted that Sazegari does not teach or suggest a combination with Barry and Priem, Barry does not teach or suggest a combination with Sazegari and Priem, and Priem does not teach or suggest a combination with Sazegari and Barry. Sazegari teaches using a permute instruction to simultaneously read data in a single table. Barry, in contrast, teaches splitting a general register file into separate address and compute register files. Priem, in contrast, teaches utilizing a system memory to store wave tables. It would be impermissible hindsight, based on Applicants own disclosure, to combine Sazegari, Barry, and Priem.

Furthermore, even if Sazegari, Barry, and Priem were combined, such a combination would lack receiving a first vector having a first plurality of numbers, each of the first plurality of numbers pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables, as recited in claim 1.

Therefore, Applicants respectfully submit that claim 1 is not obvious under 35 U.S.C. § 103(a) in over Sazegari, in view of Barry, and further in view of Priem.

Because claims 2-3, 25-27, and 49 contain the discussed limitations, Applicants respectfully submit that claims 2-3, 25-27, and 49 are not obvious under 35 U.S.C. § 103(a) in over Sazegari, in view of Barry, and further in view of Priem.

Applicants have amended claim 4 to include receiving the single instruction having an identity number code that specifies a DMA controller and a bit segment which specifies a count indicating a number of entries to be loaded in each of a plurality of look-up units.
It is respectfully submitted that Sazegari does not teach or suggest a combination with Barry and Priem, Barry does not teach or suggest a combination with Sazegari and Priem, and Priem does not teach or suggest a combination with Sazegari and Barry. Sazegari teaches using a permute instruction to simultaneously read data in a single table. Barry, in contrast, teaches splitting a general register file into separate address and compute register files. Priem, in contrast, teaches utilizing a system memory to store wave tables. It would be impermissible hindsight, based on Applicants own disclosure, to combine Sazegari, Barry, and Priem.

Furthermore, even if Sazegari, Barry, and Priem were combined, such a combination would lack the following limitations of amended claim 4: receiving the single instruction having an identity number code that specifies a DMA controller and a bit segment which specifies a count indicating a number of entries to be loaded in each of a plurality of look-up units.

Therefore, Applicants respectfully submit that claim 4 is not obvious under 35 U.S.C. § 103(a) in over Sazegari, in view of Barry, and further in view of Priem.

Because claims 5-9, and 28-33 contain the related limitations, Applicants respectfully submit that claims 5-9, and 28-33 are not obvious under 35 U.S.C. § 103(a) in over Sazegari, in view of Barry, and further in view of Priem.

Conclusion

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections of all pending claims have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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Date: 11/28/2006 By: _____

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